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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,654	09/18/2003	David Jia Chen	ROC920030233US1	8565

23334 7590 02/27/2009

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EXAMINER	
JAGER, RYAN C	
ART UNIT	PAPER NUMBER
2816	

NOTIFICATION DATE	DELIVERY MODE
02/27/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID JIA CHEN and EUGENE JAMES NOSOWICZ

Appeal 2009-0227
Application 10/665,654
Technology Center 2800

Decided:[1] February 25, 2009

Before JOSEPH F. RUGGIERO, MAHSHID D. SAADAT,
and CARLA M. KRIVAK, *Administrative Patent Judges*.

SAADAT, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's Final Rejection of claims 1-14. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Appellants' invention relates to a delay element for use in integrated circuits employing stacks of uniform minimum channel length transistors (Spec. 3-4). An understanding of the invention can be derived from a reading of representative independent claim 1, which is reproduced as follows:

> 1. A delay element, comprising:
> an input signal to be delayed; and
> a series of at least two delay stages;
> wherein each of the delay stages includes a stack of uniform channel length transistors with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that tolerances across the delay stages track tolerance of other circuits on a chip;
> wherein the use of uniform channel length transistors provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip;
> wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages;
> wherein a source of a top transistor in the stack is coupled to a first reference voltage;
> wherein a source of a bottom transistor in the stack is coupled to a second reference voltage;

> wherein a drain of the top transistor is electrically coupled to a of the drain bottom transistor in the stage so as to form an output of the stage;
>
> wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and
>
> wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

The Examiner relies on the following prior art reference:

Sato	US 5,602,798	Feb. 11, 1997

Claims 1-14 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Sato.

We make reference to the Appeal Brief (filed Sep. 10, 2007), the Reply Brief (filed Jan. 22, 2008), and the Answer (mailed Nov. 20, 2007) for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments which Appellants did not make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUE

The issue is whether the Examiner erred in rejecting the claims under 35 U.S.C. § 102(b). The issue specifically turns on whether Sato anticipates Appellants' claimed invention by disclosing a delay element having delay stages including a stack of uniform channel length transistors, as recited in claim 1.

FINDINGS OF FACT

1. Sato discloses a delay circuit for a synchronous semiconductor memory device that delays an externally applied snooze mode signal to be supplied to a clock input circuit (Abstract).

2. As depicted in Figure 10, the internal snooze mode signal generating portion includes delay elements 45a and 45b, each formed of even number of stages of cascaded CMOS inverters (col. 13, ll. 14-46).

3. Sato shows a modification of the delay element of Figure 10 in Figure 14A in the form of cascaded gate circuits 60a-60n, which have the same structure (col. 14, ll. 32-42).

4. Sato describes each of gate circuits 60a-60n as an inverter which increases the capacitance of the input node due to the number of MOS transistors connected to the input node ID1 (col. 14, ll. 44-47).

5. Sato further describes the delay resulting from large input gate capacitance and small current driving capability of the gate circuits 60a-60n (col. 14, ll. 48-61).

6. Sato compares the benefits of cascaded gate circuits with the case of using a simple CMOS inverter formed of one p-channel MOS transistor and one n-channel MOS transistor when the transistors used therein have the same size (col. 14, ll. 61-67).

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375-76 (Fed. Cir. 2005), citing

Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc., 976 F.2d 1559, 1565 (Fed. Cir. 1992). "Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) ("In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") (internal citations omitted).

ANALYSIS

Appellants argue that it is not clear as to what specific feature of the transistor is meant by the teaching of Sato related to the term "same structure" (App. Br. 13). Appellants further assert that even if the term "same structure" is used to connote "uniform channel length," Sato does not specifically disclose the uniform tolerance variations obtained from uniform channel lengths (App. Br. 13-14). The Examiner relies on Sato's teaching regarding same structure (col. 14, ll. 35-36) and same size transistors (col. 14, 65-66) to conclude that the channel lengths of such transistors are also uniform (Ans. 7). The Examiner further relies on three different references to show that "same size" transistors have the same channel lengths (*id.*). In response, Appellants contend that channel length is not specifically mentioned in Sato and further rely on a text book definition that describes a transistor size in terms of its channel width and length (Reply Br. 5).

We find that Sato provides for a delay element formed of even number of cascaded CMOS inverter stages (FF 1 and 2) wherein each stage is formed of cascaded gate circuits having the same structure (FF 3). Sato

further describes the delay mechanism and the benefits of cascaded gate circuits in the case where the transistors have the same size (FF 4-6). While, Sato does not explicitly mention "channel length" in discussing the transistors in the cascaded gate circuits 60a-60n, their characterization as transistors having the "same structure" and the "same size" (FF 3 and 6) implies that the transistors' feature dimensions are the same.

Giving the claims their broadest reasonable interpretation in light of the Specification, we find that the claimed term does not preclude uniform dimensions of the other aspects of the transistors, such as its channel width. This interpretation is consistent with Appellants' purported definition (Reply Br. 5) of a transistor "size" as determined by the transistor's channel width *and* length. Therefore, while Appellants' claims require at least uniform channel length, Sato's transistors are implied to have uniformity in other dimensions in addition to their channel length. Based on the breadth of the recited language in claim 1 and the teachings of Sato, we disagree with Appellants' argument that the same structure and size stacked transistors disclosed by Sato do not have uniform channel lengths.

With respect to the claimed uniform tolerance variations resulting from uniform channel length transistors, we further agree with the Examiner and find that using the same structure and size transistors of Sato results in uniform tolerance variations across the other circuits. Appellants' delay element, to the extent disclosed, provides such uniformity in tolerance variations merely by using uniform channel length transistors. Therefore, the claimed uniform tolerance variation also results from the delay element of Sato, which has identical characteristics.

CONCLUSION

On the record before us, Appellants have failed to show that the Examiner erred in rejecting claims 1-14. Therefore, since Sato anticipates Appellants' claimed invention by disclosing a delay element having delay stages including a stack of uniform channel length transistors, we sustain the 35 U.S.C. § 102(b) rejection of claim 1, as well as claims 2-14 which are argued together as one group (App. Br. 16), over Sato.

ORDER

In view of our analysis above, we affirm the Examiner's decision to reject claims 1-14.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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